深圳市雅创芯瀚电子科技有限公司
SHENZHEN ASTRONG-TECH CO., LTD

eMMC 存储芯片

数据手册

服务电话：19070202259　13691641629

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1、简介

eMMC 是一种嵌入式闪存存储解决方案。它结合了嵌入式闪存控制器，包括基于 LDPC 的 ECC 和闪存，以及 JEDEC 标准 eMMC 5.1 接口。eMMC 控制器（包括基于 LDPC 的 ECC）指导闪存管理，包括 ECC、磨损均衡、IOPS 优化，显著降低主机 CPU 的存储管理负担。

eMMC 是许多电子设备的理想存储解决方案。eMMC 的设计涵盖了广泛的应用领域，如智能手机、平板电脑、移动电话、PDA、手持电子设备、数码摄像机、多媒体设备等。以其紧凑的体积、低功耗和许多增强的特性不仅用于消费产品，在嵌入式应用中同样得到了快速广泛的应用，诸如大量计算机端的模块设计。

2、订货信息

表 1 订货信息和配置

容量	型号	Flash 类型	工作温度	封装类型
8GB	ASTCE-008GSN	pSLC	-55℃~125℃	153FBGA
16GB	ASTCE-016GSN			
32GB	ASTCE-032GSN			
64GB	ASTCE-064GSN			
8GB	ASTCE-008GSE	pSLC	-55℃~105℃	
16GB	ASTCE-016GSE			
32GB	ASTCE-032GSE			
64GB	ASTCE-064GSE			
64GB	ASTCE-064GTI	TLC	-55℃~95℃	
128GB	ASTCE-128GTI			
256GB	ASTCE-256GTI			

3、产品特性

- 遵循 eMMC5.1 标准；
- 支持 3.3V/1.8V 电源；
- 支持 12 线总线（CLK、CMD、数据选通、数据总线和 RST_n）；
- 高达 400MHz 的时钟速度；
- 支持单数据速率（SDR）和双数据速率（DDR）；
- 支持不同的总线宽度：1 位、4 位、8 位；
- 支持 RPMB；
- 支持具有增强属性的多个分区；
- 支持锁定/解锁和写保护；
- 支持电源故障的数据保护；
- 擦写次数：pSLC类型 6万次，TLC类型 3000次
- 断电保持时间：10年(10%擦写次数)/1年(100%擦写次数)

- 支持高优先级中断（HPI）；
- 支持动态电源管理器：待机和睡眠模式；
- 支持命令队列；
- 支持安全写保护；

3.1 产品性能

表 2 产品性能

容量	型号	连续读取性能(MB/s)	连续写入性能(MB/s)
8GB	ASTCE-008GSN	275	136
16GB	ASTCE-016GSN	275	136
32GB	ASTCE-032GSN	290	223
64GB	ASTCE-064GSN	275	174
8GB	ASTCE-008GSE	275	136
16GB	ASTCE-016GSE	275	136
32GB	ASTCE-032GSE	290	223
64GB	ASTCE-064GSE	275	174
64GB	ASTCE-064GTI	232	167
128GB	ASTCE-128GTI	290	217
256GB	ASTCE-256GTI	267	198

3.2 物理特性

3.2.1 FBGA153 封装

- 物理尺寸：11.5mm x 13.0mm x 1mm；

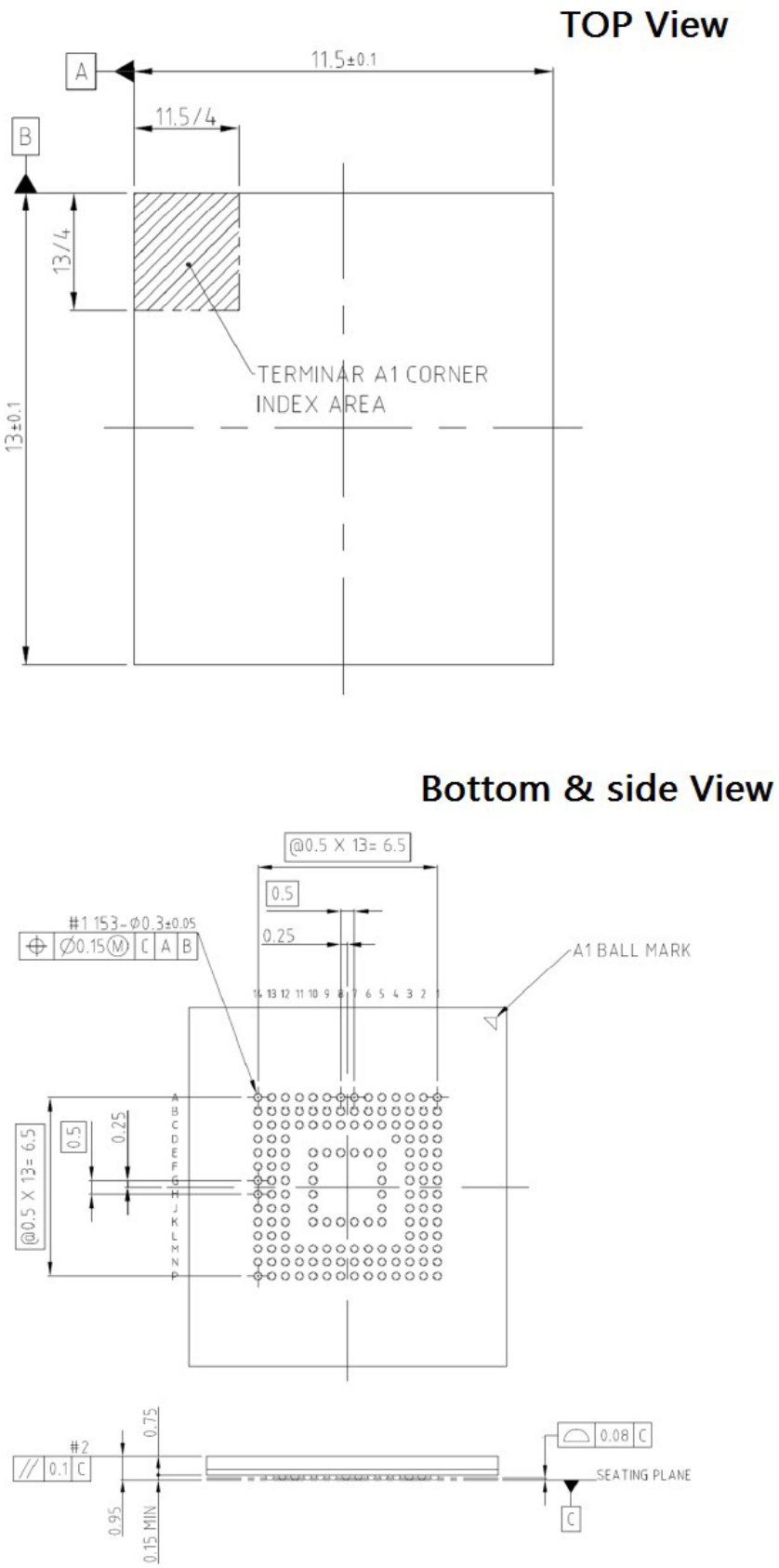
TOP View
A
11.5±0.1
11.5/4
B
13/4
13±0.1
TERMINAR A1 CORNER
INDEX AREA
Bottom & side View
@0.5 X 13= 6.5
0.5
0.25
#1 153-Ø0.3±0.05
Ø0.15 M C A B
A1 BALL MARK
14 13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P
@0.5 X 13= 6.5
0.5
0.25
#2
0.1 C
0.75
0.95
0.15 MIN
0.08 C
SEATING PLANE
C

图 1 物理封装图

- 引脚定义

引脚图按照 TopView 如下所示：

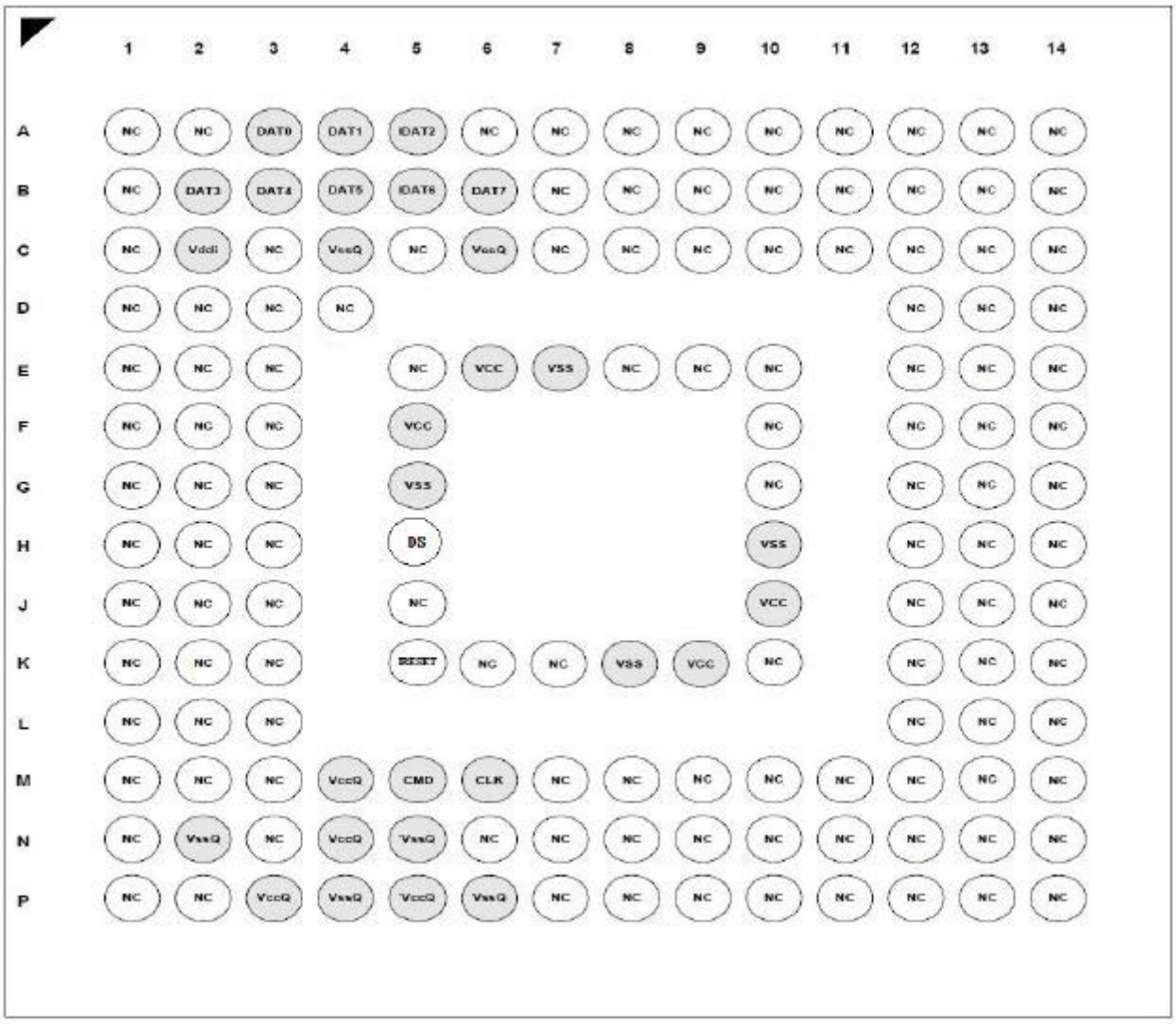

图 2 引脚定义图

- 引脚信号描述

表 3 引脚信号描述

153-Ball Device	Symbol	Type	Ball Function
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfer. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.

A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
K5	RST_n	Input	Reset signal pin
E6, F5, J10, K9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
C6, M4, N4, P3, P5	VccQ	Supply	VccQ: Memory controller core and MMC interface I/O power supply.
E7, G5, H10, K8	VSS	Supply	Vss: Flash memory I/F and Flash memory ground connection.
C4, N2, N5, P4, P6	VssQ	Supply	VssQ
C2	VDDi		VDDi : Connect 1uF capacitor from VDDi to ground.
H5	DS		Data Strobe: Return clock signal used in HS400 mode

3.3 电气特性

- 工作电压范围：

  VCC = 2.7V~3.6V (typical 3.3V)；

  VCCQ = 1.7V~1.95V(typical 1.8V), 2.7V~3.6V (typical 3.3V)；

- 工作温度：

  工业级：-40~85℃；

  宽温工业级：-55~105℃；

  军工级：-55~125℃；

  无操作存储温度：-55~125℃。

- 其他

  符合 ROHS。

4、功能框图

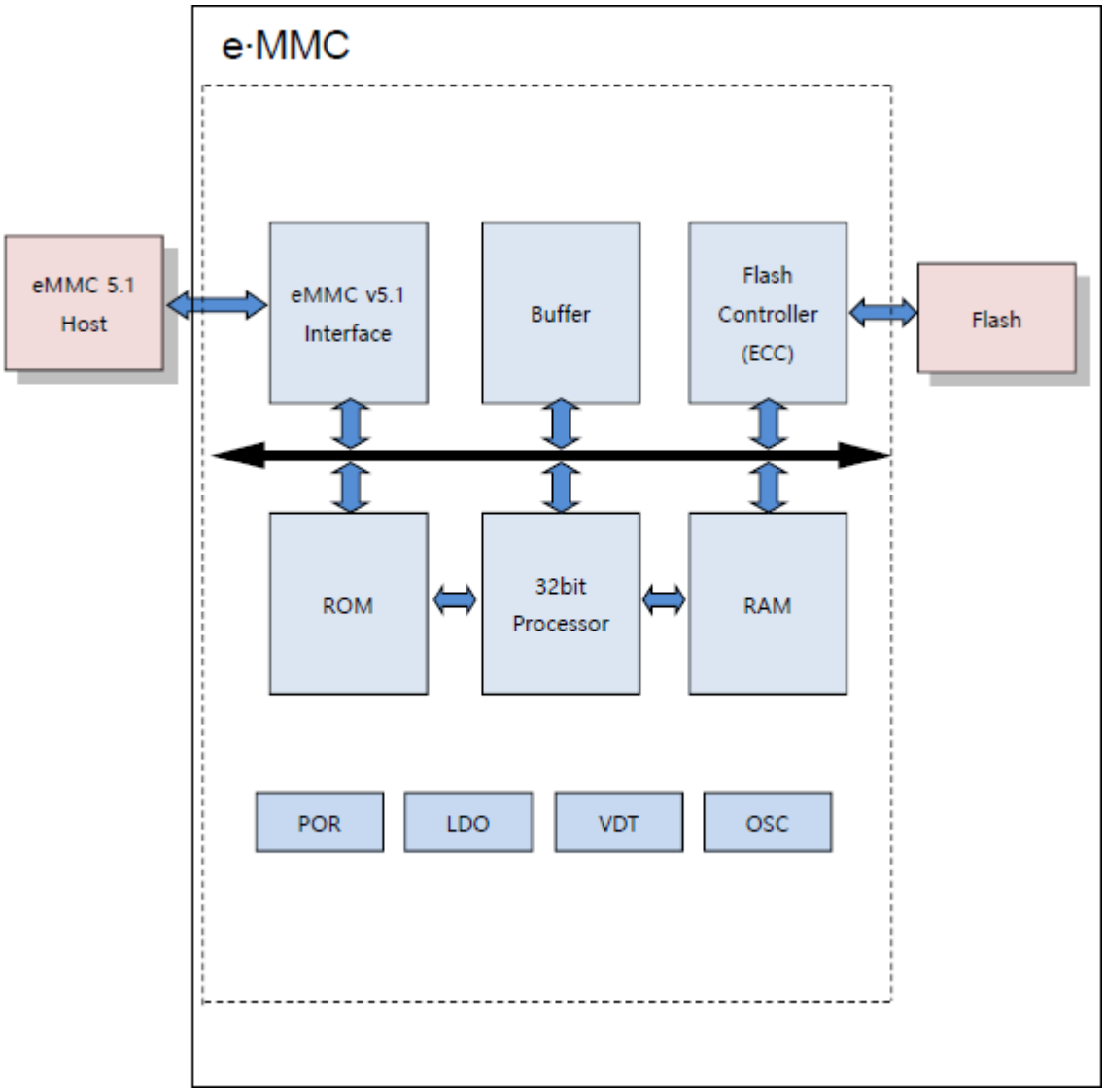

图 3 芯片功能框图

5、eMMC的系统框架

5.1 eMMC的主设备系统框图

eMMC 主从设备互联框架图，如图所示。

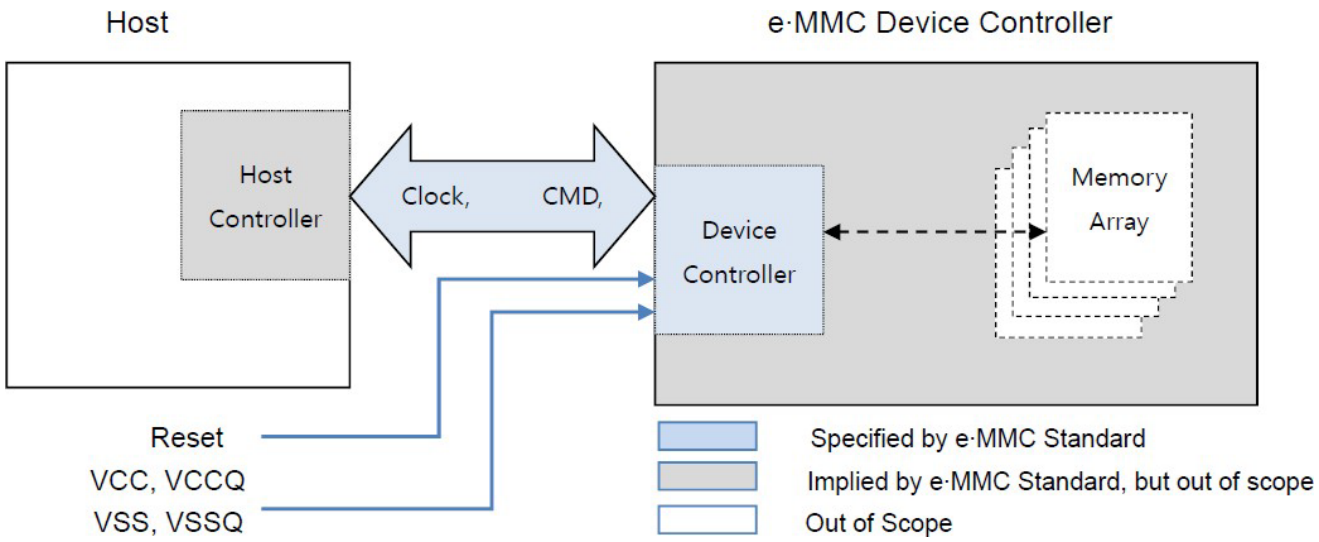

图 4 主从设备连接框图

5.2 eMMC的从设备简介

eMMC 总线分别为以下数据和电源线；

CLK：时钟输入；

DS：在HS400模式下用于输出的数据选通；

CMD：命令是一个双向信号。主设备和 eMMC 在两种模式下工作，开路和上拉；

DAT0~DAT7：数据线是双向信号。Host 端和 eMMC 在上拉状态下进行操作；

RST_n：硬件复位输入；

VCC：是核心电压和 flash IO 的供电电压；

VCCQ：是主机接口的供电电源；

VSSQ：地线。

表 4 e MMC 接口一览表

Name	Type	Description
CLK	I	Clock
DS	O/PP	Data Strobe
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
I: input, O: output, PP: push-pull, OD: open-drain, NC: Not connected, S: power supply		

表 5 e MMC 寄存器一览表

Name	Width (bytes)	Description
CID	16	Device Identification number, an individual number for Identification.
RCA	2	Relative Device Address, is the device system address, Dynamically assigned by the host during initialization.
DSR	2	Driver stage Resister, to configure the Device's output drivers.
CSD	16	Device Specific Data, information about the Device operation Conditions.
OCR	4	Operation Conditions Resister. Used by a special broadcast command to identify the voltage type of the Device.
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0

6、eMMC5.1 特性

6.1 Boot

eMMC 支持 JESD84-B51A 引导操作模式，支持强制模式和备用模式。

6.2 休眠模式

设备可以通过睡眠/唤醒（CMD 5）在睡眠状态和待机状态之间切换。在睡眠状态下，存储设备的功耗最小化。在此状态下，内存设备仅对命令 RESET（参数为 0x00 000000 或 0XF0F0F-0f0 或 H/W RESET 的 CMD0）和 SLEEP/AWEAK（CMD5）做出反应。内存设备会忽略所有其他命令。Vcc 电源可能在睡眠状态下关闭，以便进一步节省系统功耗。

有关更多信息，请参考 JESD84-B51A。

6.3 总线模式

- 启动模式

在电源循环、接收到参数为 0xF0 的 CMD0 或硬件重置信号的断言后，设备将处于引导模式。

- 设备识别模式

引导操作模式完成后，或者主机和/或设备不支持引导操作模式时，设备将处于设备识别模式。设备将处于此模式，直到收到 SET_RCA co 命令（CMD3）。

- 中断模式

主机和设备同时进入和退出中断模式。在中断模式下，没有数据转换器。唯一允许的消息是来自设备或主机的中断服务请求。

- 数据传输模式

一旦分配了 RCA，设备将进入数据传输模式。在总线上识别设备后，主机将进入数据传输模式。

- 非活动模式

如果设备工作电压范围或访问模式无效，设备将进入非活动模式。设备还可以使用 GO_inactive_STATE 命令（CMD15）进入非活动模式。设备将在通电后重置为预空闲状态。

表 6 总线模式一览表

Device State	Operation mode	Bus mode
Inactive State	Inactive mode	Open-drain
Pre-Idle State	Boot mode	
Pre-Boot State		
Idle State	Device identification mode	
Identification State		
Stand-by State		
Sleep State	Data transfer mode	Push-pull
Transfer State		
Bus-Test State		
Sending-data State		
Receive-data State		
Programming State		
Disconnect State		
Boot State	Boot mode	
Wait-IRQ State	Interrupt mode	Open-drain

6.4 可靠写入

按照 eMMC 5.1 规范要求，eMMC 支持 512 字节可靠写入。

可靠写入是一种特殊的写入模式，其中逻辑地址指向的旧数据必须保持不变，直到写入同一逻辑地址的新数据成功编程。这是为了确保可靠写入后，目标地址在做数据更新时不会包含未定义的数据。当执行可靠写入时，即使编程过程中突然断电，数据也将保持有效。

6.5 安全擦除

除了标准的擦除命令外，eMMC 支持可选的安全擦除命令。

安全擦除命令与基本擦除命令的不同之处在于，它要求设备和主机在移动到下一个设备操作之前等待操作完成。

有关更多信息，请参考 JESD84-B51A。

安全擦除命令要求设备对擦除组执行安全清除操作，并在这些擦除组中复制标识为要擦除的项目。清除操作定义为用单个字符覆盖可寻址位置并执行擦除。

这个新命令满足了高安全性应用程序的要求，即一旦数据被擦除，就不能再从设备中检索数据。

6.6 Trim

Trim 功能与 Erase 命令类似，但将 Erase 操作应用于写入块，而不是擦除组。

有关更多信息，请参考 JESD84-B51A。

6.7 分区管理

从设备的默认区域包括一个用于存储数据的用户数据区域、两个用于引导的可能引导区域分区，以及一个用于以经过身份验证和保护的 RPMB 分区。内存配置初始包括（在任何分区操作之前）用户数据区、RPMB 区分区和引导区分区。

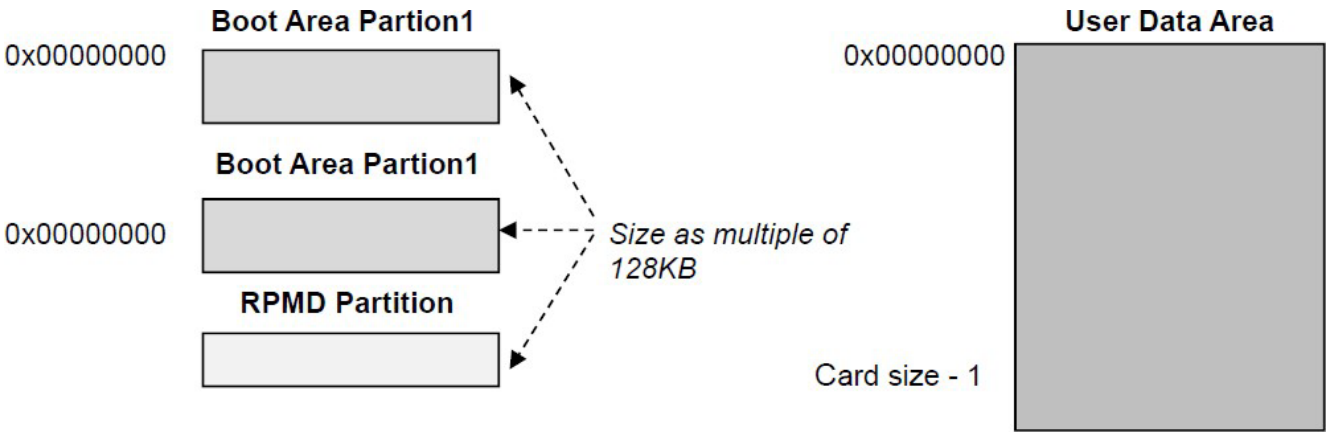

图 5 分区管理图

6.8 高优先级中断（HPI）

许多操作系统使用请求分页来启动用户请求的进程。如果主机需要在连线操作过程中获取页面，则请求将被延迟，直到写入命令完成，在最坏的情况下，这可能需要 350 毫秒。

JESD84-B51A 中定义的高优先级中断（HPI）通过在低优先级操作实际完成之前暂停低优先级操作来实现低读取延迟操作。这种机制可以将典型情况下的读取延迟减少到 5 毫秒。

有关更多信息，请参考 JESD84-B51A。

6.9 后台操作

设备需要在内部执行各种维护操作，例如收集、擦除和压缩。为了减少时间关键型操作期间的延迟，最好在设备不为主机服务时执行维护操作。

然后将操作分为两种类型：前台操作（如读或写命令）和后台操作（设备在主机未被服务时可以执行的操

作）。

有关更多信息，请参考 JESD84-B51A。

6.10 H/W 复位

主机可以使用硬件复位来重置设备，在设备重置之前将复位引脚置预空闲状态，对上电写保护的块进行使能关闭。

6.11 缓存

缓存是 eMMC 设备中的临时存储空间。在典型情况下，高速缓存应该减少写入和读取的访问时间。主机无法直接访问缓存。该缓存还可用于一些特定的操作，例如作为基于 LDPC 纠错算法的存储器控制器的执行存储器和/或作为地址映射表等的存储器，但其定义超出本规范的范围。

有关更多信息，请参考 JESD84-B51A。

6.12 动态容量管理

大量内存使用和闪存老化可能会导致坏块。动态容量管理为存储设备提供了一种减少其重复性的机制提高容量，延长设备寿命。

操作动态容量的机制基于：内存阵列分区和 WP 组的粒度。通过在用户区域的地址空间内释放任何 WP 组来降低容量。一个已发布的 WP 组将作为一个永久写保护组，不应从中读取：写入一个已发布的 WP 组内的地址会返回一个 WP 错误；读取已发布 WP 组的地址标题时，可能会返回错误；检查写保护（使用 CMD30）和写保护类型（使用 CMD31）时，应相应地报告受保护组和永久写保护。

有关更多信息，请参考 JESD84-B51A。

7 寄存器

7.1 OCR 寄存器

32 位操作条件寄存器（Operation Conditions Register ，OCR）存储设备的 VDD电压和访问模式信息。此外，该寄存器还包括状态信息位。如果设备启动过程已经完成，此状态位就会被设置。所有设备均支持OCR。

表 7 OCR 寄存器状态表

OCR bit	Description	Value	Remark
[6:0]	Reserved	000 0000b	
[7]	1.70 ~ 1.95V	1b	
[14:8]	2.0 ~ 2.6V	000 0000b	
[23:15]	2.7 ~ 3.6V	1 1111 1111b	
[28:24]	Reserved	0 0000b	

[30:29]	Access mode	10b	
[31]	card power up status bit (busy)1		

注: 【31】如果设备尚未完成通电程序，则该位设置为低。

7.2 CID 寄存器

CID Register 是设备识别寄存器，它是一个128 位宽的寄存器。包含设备识别阶段（协议）中使用的设备识别信息。每一个闪存或I/O 设备，都应该有一个唯一的识别码。eMMC 设备具有唯一的识别码（CID）。下表列出了 eMMC 产品的设备识别寄存器结构定义。。

表 8 CID 寄存器状态表

Name	Field	Width	CID-Slice	CID Value	Remark
Manufacture ID	MID	8	[127:120]	FFh	
Reserved		6	[119:114]		
Card / BGA	CBX	2	[113:112]	01	BGA
OEM/Application ID	OID	8	[111:104]	FFh	Not fixed
Product name	PNM	48	[103:56]	FFFFFFh	
Product revision	PRV	8	[55:48]	FFh	Not fixed
Product serial number	PSN	32	[47:16]	Randomby Production	Not fixed
Manufacturing date	MDT	8	[15:8]	month，year	Not fixed
CRC7 checksum	CRC	7	[7:1]	00h	Not fixed
Not used, always ‘1’	-	1	[0:0]	1h	

7.3 CSD 寄存器

CSD（Card-Specific Data)寄存器提供如何访问 eMMC 内容的信息。该寄存器定义了数据格式、纠错类型、最大数据访问时间、数据传输速度、 DSR 寄存器是否可用等信息。寄存器的可编程部分（以 W 或 E 标记的条目，见下文）可由 CMD27 更改。表格中条目类型编码如下:

R: Read only

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.;

表 9 CSD 寄存器状态表

Name	**Field**	**Width**	**Cell t ype**	**CSD Slice**	**CSD Value**	**Remark**
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System Specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved	-	2	R	[121:120]		
Data read access-time 1	TAAC	8	R	[119:112]	2Fh	20ms
Data read access-time 2in CLK cycle (NSAC*100)	NSAC	8	R	[111:104]	1h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	2Ah	20MHz
Device command classes	CCC	12	R	[95:84]	5F5h	Class 0, 2,4,5,6,7, 8,10
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	512B
Partial blocks for read allowe d	READ_BL_PARTIAL	1	R	[79:79]	0h	Not suppor t
Write block misalignment	WIRTE_BLK_MISALIGN	1	R	[78:78]	0h	Not suppor t
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	Not suppor t
DSR implemented	DSR_IMP	1	R	[76:76]	0h	Not suppor t
Reserved		2	R	[75:74]		
Device size	C_SIZE	12	R	[73:62]	FFFh	
Max read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]	6h	
Max read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]	6h	
Max write current @VDD min	VDD_W_CURR_MIN	3	R	[53:53]	6h	
Max write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]	6h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	1h	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Write speed factor	R2W_FACTOR	3	R	[28:26]	1h	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	512B
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	Not suppor t

Reserved		4	R	[20:17]		
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	Not suppor t
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	None
CRC	CRC	7	R/W/E	[7:1]	Dh	
Not used, always'1'		1	-	[0:0]	1h	

以下部分介绍 CSD 字段和相关数据类型。如果没有明确定义，则所有位字符串都被解释为从左位开始的二进制编码数字。

7.4 扩展 CSD 寄存器

扩展 CSD （Extended CSD）寄存器定义了 eMMC 属性和选定模式，长度为 512 字节。高位的 320 字节是属性字段，它定义了 eMMC 容量，主机不能修改。低位的 192 个字节是模式字段，它定义了 eMMC 正在使用的配置。主机可以通过 SWITCH 命令修改这些配置。

R: Read only

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and

readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

表 10 扩展 CSD 寄存器状态表

Name	Field	Cell type	CSD Slice	EXT_CSD Value	Remark

Properties Segment					
Reserved1	RESERVED	TBD	[511:506]		
Extended Security Command Error	EXT_SECURITY_ER R	R	[505]	0h	Only for eMMC4.5 by JESD84-B51A
Supported Command Sets	S_CMD_SET	R	[504]	1h	Allocated by MMCA
HPI features	HPI_FEATURES	R	[503]	3h	Bit[1]=1: HPI mechanism implementation base on CMD12 Bit[1]=0: HPI mechanism implementation base on CMD13 Bit[0]=1: HPI mechanism support Bit[0]=0: HPI mechanism not support (default)
Background operations support	BKOPS_SUPPORT	R	[502]	1h	Background operation are supported
Max packed read commands	MAX_PACKED_READS	R	[501]	3Fh	
Max packed write commands	MAX_PACKED_WRITE S	R	[500]	3Fh	
Data Tag Support	DATA_TAG_SUPPO RT	R	[499]	1h	System data tag supported
Tag Unit Size	TAG_UNIT_SIZE	R	[498]	1h	1024Bytes
Tag Resources Size	TAG_RES_SIZE	R	[497]	0h	
Context Management Capabilities	CONTEXT_CAPABILITI ES	R	[496]	5h	
Large Unit Size	LARGE_UNIT_SIZE_M 1	R	[495]	0h	
Extended partition Attribute Support	EXT_SUPPORT	R	[494]	3h	
Supported modes	SUPPORTED_MOD ES	R	[493]	1h	
FFU features	FFU_FEATURES	R	[492]	1h	
Operation codes timeout	OPERATION_CODE_TI MEOUT	R	[491]	17h	
FFU Argument	FFU_ARG	R	[490:487]	0h	
Barrier support	BARRIER_SUPPOR T	R	[486]	0h	
Reserved1		TBD	[485:309]		
CMD Queuing Support	CMDQ_SUPPORT	R	[308]	0h	
CMD Queuing Depth	CMDQ_DEPTH	R	[307]	0h	
Reserved1		TBD	[306]		
Number of FW sectors correctly programmed	NUMBER_OF_FW_SE CTORS_CORRECTLY_P ROGRAMM ED	R	[305:302]	0h	
Vendor proprietary health report	VENDOR_PROPRIETA RY_HEALTH_RE PORT	R	[301:270]	0h	

Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	R	[269]	1h	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	R	[268]	1h	
Pre EOL information	PRE_EOL_INFO	R	[267]	1h	
Optimal read size	OPTIMAL_READ_SIZE	R	[266]	8h	
Optimal write size	OPTIMAL_WRITE_SIZE	R	[265]	8h	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	R	[264]	8h	
Device version	DEVICE_VERSION	R	[263:262]	0h	
Firmware version	FIRMWARE_VERSION	R	[261:254]	---	
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	R	[253]	0h	
Cache size	CACHE_SIZE	R	[252:249]	100h	
Generic CMD6 timeout	GENERIC_CMD5_TIME	R	[248]	32h	Not defined
Power off notification (long)timeout	POWER_OFF_LONG_TIME	R	[247]	3Ch	Not defined
Background operations status	BKOPS_STATUS	R	[246]	0h	Outstanding : No operation required
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	R	[245:242]	0h	
1st initialization time after partitioning	INI_TIMEOUT_AP	R	[241]	1Eh	Initial time out 3s
Cache Flushing Policy	CACHE_FLUSH_POLICY	R	[240]	0h	
Power class for 52MHz, DDR at VCC = 3.6V	PWR_CL_DDR_52_360	R	[239]	0h	
Power class for 52MHz, DDR at VCC = 1.95V	PWR_CL_DDR_52_195	R	[238]	0h	
Power class for 200MHz at VCCQ = 1.95V, VCC = 3.6V	PWR_CL_200_195	R	[237]	0h	
Power class for 200MHz at VCCQ = 1.3V, VCC = 3.6V	PWR_CL_200_130	R	[236]	0h	
Minimum Write Performance for 8bit At 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	R	[235]	0h	
Minimum Read Performance for 8bit At 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	R	[234]	0h	
Reserved1	RESERVED	TBD	[233]		
TRIM Multiplier	TRIM_MULT	R	[232]	2h	TRIM Timeout =300ms*2=600ms

Secure Feature support	SEC_FEATURE_SUPPORT	R	[231]	55h	Support the sanitize operation Support the secure and insecure trim operation Support the auto erase on retired defective portion of array Secure purge operations are supported
Secure Erase Multiplier	SEC_ERASE_MULT	R	[230]	1Bh	Secure Erase Timeout= 5.1 sec
Secure TRIM Multiplier	SEC_TRIM_MULT	R	[229]	11h	Secure trim Timeout= 8.1 sec
Boot information	BOOT_INFO	R	[228]	7h	Bit[2]=1: Device supports high speed timin g during boot Bit[1]=1: Device supports dual data rate d uring boot Bit[0]=1: Device supports alternate boot m ethod Bit[0,1,2]=0: Not supports each feature Bit[7:3=Reserved
Reserved1	RESERVED	TBD	[227]		
Boot partition size	BOOT_SIZE_MULT	R	[226]	20h	
Access size	ACC_SIZE	R	[225]	6h	
High-capacity erase unit size	HC_ERASE_GRP_S IZE	R	[224]	1h	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	R	[223]	1h	High Capacity erase timeout: 300ms
Reliable write sector count	REL_WR_SEC_C	R	[222]	1h	1sector
High-capacity write protect group size	HC_WP_GRP_SIZE	R	[221]	20h	
Sleep current (VCC)	S_C_VCC	R	[220]	7h	Sleep Current :128uA
Sleep current(VCCQ)	S_C_VCCQ	R	[219]	7h	Sleep Current :128uA
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	R	[218]	17h	
Sleep/awake timeout	S_A_TIMEOUT	R	[217]	17h	Sleep/Awake Timeout : 85ms
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	R	[216]	11h	
Sector Count	SEC_COUNT	R	[215:212]	---	64GB : 747C000h
Secure Write Protect Information	SECURE_WP_INFO	TBD	[211]	0h	

Minimum Write Performance for 8bit At 52MHz	MIN_PERF_W_8_52	R	[210]	0h	
Minimum Read Performance for 8bit At 52MHz	MIN_PERF_R_8_52	R	[209]	0h	
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	R	[208]	0h	
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	R	[207]	0h	
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	R	[206]	0h	
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_R_26	R	[205]	0h	
Reserved1	RESERVED	R	[204]		
Power class for 26MHz at 3.6V 1R	PWR_CL_26_360	R	[203]	0h	MAX RMS Current = 100mA, MAX Peak Current = 200mA
Power class for 52MHz at 3.6V 1R	PWR_CL_52_360	R	[202]	0h	MAX RMS Current = 100mA, MAX Peak Current = 200mA
Power class for 26MHz at 1.95V 1R	PWR_CL_26_195	R	[201]	0h	MAX RMS Current = 65mA, MAX Peak Current = 130mA
Power class for 52MHz at 1.95V 1R	PWR_CL_52_195	R	[200]	0h	MAX RMS Current = 65mA, MAX Peak Current = 130mA
Partition switching timing	PARTITION_SWITCH_TIME	R	[199]	5h	Partition switch time : 10ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	R	[198]	19h	HPI time out : 20ms
I/O Driver Strength	DRIVER_STRENGT H	R	[197]	Fh	Support driver strength Type0,1,2,3
Device type	DEVICE_TYPE	R	[196]	57h	1. HS400 @1.8V High-speed Data Rate 52@1.8V/3.3V High-speed Data Rate 52@rated device voltage(s) High-speed Data Rate 26@rated device voltage(s)
Reserved1	RESERVED	TBD	[195]		

CSD structure	CSD_STRUCTURE	R	[194]	2h	CSD version No.1.2
Reserved1	RESERVED	TBD	[193]		
Extend CSD revision	EXT_CSD_REV	R	[192]	8h	Revision 1.8(for MMC v5.1)
Modes Segment					
Command set	CMD_SET	R/W/E_P	[191]	0h	
Reserved1	RESERVED	TBD	[190]		
Command set revision	CMD_SET_REV	R	[189]	0h	V4.0
Reserved1	RESERVED	TBD	[188]		
Power class	POWER_CLASS	R/W/E_P	[187]	0h	See EXT_CSD in spec.
Reserved1	RESERVED	TBD	[186]		
High-speed interface timing	HS_TIMING	R/W/ E_P	[185]	0h	It depends on Host I/F speed. Default is 0, But it can be 1 by host
Strobe Support	STROBE_SUPPORT	R	[184]	1h	
Bus width mode	BUS_WIDTH	W / E_P	[183]	0h	
Reserved1	RESERVED		[182]		
Erase memory content	ERASED_MEM_CO NT	R	[181]	0h	0 after erase
Reserved1	RESERVED	TBD	[180]		
Partition configuration	PARTITION_CONFI G	R/W/ E & R/ W/E_P	[179]	0h	
Boot config protection	BOOT_CONFIG_PROT	R/W/ E & R/ W/C_P	[178]	0h	
Boot bus Conditions	BOOT_BUS_CONDITIO NS	R/W/E	[177]	0h	
Reserved1	RESERVED	TBD	[176]		
High-density erase group definition	ERASE_GROUP_D EF	R	[175]	0h	
Boot write protection status registers		TBD	[174]	0h	

Boot area write protection register	BOOT_WP	R/W/ E & R/ W/C_P	[173]	0h	Bit[6]=0 : Master is permitted to set B_P WR_WP_EN (bit0) Bit[4]=0 : Master is permitted to set B_PE RM_WP_EN (bit2) Bit[2]=0 : Boot Region is not permanently write protected Bit[0]=0: Boot Region is not power-on write protected
Reserved1	RESERVED	TBD	[172]		
User area write protection register	USER_WP	R/W, & R/ W/C_P & RW/E_P	[171]	0h	
Reserved1	RESERVED	TBD	[170]		
FW configuration	FW_CONFIG	R/W	[169]	0h	FW updates enabled
RPMB Size	RPMB_SIZE_MULT	R	[168]	20h	RPMB size 512KB
Write reliability setting register	WR_REL_SET	R/W	[167]	0h	
Write reliability parameter register	WR_REL_PARAM	R	[166]	14h	Enhanced definition of reliable write All the WR_DATA_REL parameter in the WR_REL_SEL register are R/W
Start Sanitize operation	SANITIZE_START	W/E_P	[165]	0h	
Manually start background operations	BKOPS_EN	W/E _P	[164]	0h	
Enable background operations handshake	BKOPS_EN	R/W	[163]	0h	
H/W reset function	RST_n_FUNCTION	R/W	[162]	0h	
HPI management	HPI_MGMT	R/W/E_P	[161]	0h	
Partitioning Support	PARTITIONING_SU PPORT	R	[160]	7h	Can have extended partitions attribute Can have enhanced technological features Device supports partitioning features
Max Enhanced Area Size	MAX_ENH_SIZE_M ULT	R	[159:157]		32GB : 254h 64GB : 4C9h

Partitions attribute	PARTITIONS_ATTR UBUTE	R/W	[156]	0h	Bit[7:5]: Reserved Bit[4]=1: Set Enhanced attribute in General Purpose partition 4 Bit[3]=1: Set Enhanced attribute in General Purpose partition 3 Bit[2]=1: Set Enhanced attribute in General Purpose partition 2 Bit[1]=1: Set Enhanced attribute in General Purpose partition 1
Partitioning Setting	PARTITON_SETTIN G_ COMPLETED	R/W	[155]	0h	
General Purpose Partition Size	GP_SIZE_MULT	R/W	[154:143]	0h	
Enhanced User Data Area Size	ENH_SIZE_MULT	R/W	[142:140]	0h	
Enhanced User Data Start Address	ENH_START_ADDR	R/W	[139:136]	0h	
Reserved1	RESERVED	TBD	[135]		
Bad Block Management mode	SEC_BAD_BLK_MGM NT	R/W	[134]	0h	
Production state awareness	PRODUCTION_STAT_ AWARENESS	R/W/E	[133]	0h	
Package Case Temperature is Controlled	TCASE_SUPPORT	W/E_P	[132]	0h	
Periodic Wake-up	PERIODIC_WAKEU P	R/W/E	[131]	0h	
Program CID/CSD in DDR mode Support	PROGRAM_CID_CS D_DDR_SUPPORT	R	[130]	1h	
Reserved1	RESERVED	TBD	[129:128]		
Vendor Specific Fields	VENDOR_SPECIFIC_FI ELD		[127:64]	0h	
Native sector size	NATIVE_SECTOR_SIZE	R	[63]	0h	
Sector size emulation	USE_NATIVE_SECT OR	R/W	[62]	0h	
Sector size	DATA_SECTOR_SIZ E	R	[61]	0h	
1st initialization after Disabling sector size emulation	INI_TIMEOUT_EMU	R	[60]	0h	
Class 6 commands control	CLASS_6_CTRL	R/W/E_P	[59]	0h	

Number of addressed group to be Released	DYNCAP_NEEDED	R	[58]	0h	
Exception event control	EXCEPTION_EVENTS_CTRL	R/W/E_P	[57:56]	0h	
Exception event status	EXCEPTION_EVENTS_STATUS	R	[55:54]	0h	
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	R/W	[53:52]	0h	
Context configuration	CONTEXT_CONF	R/W/E_P	[51:37]	0h	
Packed command status	PACKED_COMMAND_STATUS	R	[36]	0h	
Packed command failure index	PACKED_FAILURE_INDEX	R	[35]	0h	
Power Off Notification	POWER_OFF_NOTIFICATION	R/W/E_P	[34]	0h	Power off notification is not supported by host, device should not assume any notification
Control to turn the Cache ON/OFF	CACHE_CTRL	R/W/E_P	[33]	0h	
Flushing of the cache	FLUSH_CACHE	W/E_P	[32]	0h	
Control to turn the Barrier ON/OFF	BARRIER_CTRL	R/W	[31]	0h	
Mode config	MODE_CONFIG	R/W/E_P	[30]	0h	
Mode operation codes	MODE_OPERATION_CODES	W/E_P	[29]	0h	
Reserved1		TBD	[28:27]		
FFU status	FFU_STATUS	R	[26]	0h	
Pre loading data size	PRE_LOADING_DATA_SIZE	R/W/E_P	[25:22]	0h	
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	R	[21:18]		64GB : 2648000h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	R/W/E & R	[17]	3h	
Secure Removal Type	SECURE_REMOVAL_TYPE	R/W/E & R	[16]	9h	
Command Queue Mode Enable	CMDQ_MODE_EN	R/W/E_P	[15]	0h	
Reserved1		TBD	[14:0]		
NOTE1. Reserved bits should read as “0” NOTE2. Obsolete values should be don’t care					